1. (Amended) A memory module controller for [interfacing a plurality of memory device on a memory module with a system memory bus coupled to a system memory module, the memory module controller] providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:

first interface circuitry configured to receive from the system memory [bus] controller a first memory transaction [having] in a first format; and

control logic coupled to the first interface circuitry and configured to convert the first memory transaction into [generating] a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction [corresponds to the first memory transaction and has a second format] is different [than] from the first format of the first memory transaction.

2. (Amended) The memory module controller of claim 1, further comprising:

second interface circuitry coupled to the control logic and configured to transmit the second memory transaction to at least one of the plurality of memory devices.

3. (Amended) The memory module controller of claim 1, wherein the first memory transaction includes time multiplexed address and command information.

4. (Amended) The memory module controller of claim 3, wherein the first interface circuitry comprises:

request handling logic [that separates] configured to separate the address and command information and [provides] to provide the separate address and command information to the control logic.

5. (Amended) The memory module controller of claim 4, wherein the first memory transaction further includes time multiplexed data information, and wherein the request handling logic is further configured to separate the time multiplexed data information and [provides] to provide the [separate] separated time multiplexed data information to the control logic.

6. (Amended) The memory module controller of claim 1, wherein the first interface circuitry comprises:

handshaking logic configured to provide [provides] a handshake signal to the system memory [bus] controller that indicates when the memory module controller is communicating data to the system memory [bus] controller.

7. (Amended) The memory module controller of claim 1, wherein the first interface circuitry comprises:

data handling logic configured to receive data [of] for the first memory transaction from the system memory [bus] controller and reformat the data for the second memory transaction.

8. (Amended) The memory module controller of claim 1, further comprising:

a write buffer coupled to the first interface circuitry and configured to store [storing] data sent with the first memory transaction.

9. (Amended) The memory module controller of claim 8, further comprising:

an address storage unit coupled to the write buffer and the first interface circuitry[,] and the address storage unit is configured to store [storing] addresses associated with the [write] data stored in the write buffer.

10. (Amended) The memory module controller of claim 1, further comprising:

a read buffer coupled to the control logic[, the read buffer] and configured to store [storing] data read from at least one of the plurality of memory devices.

11. (Amended) The memory module controller of claim 1, further comprising:

a clock generator circuit coupled to the control logic and configured to receive a first clock signal from the system memory [bus] controller[, the clock generator circuit generating] and to generate a second clock signal for the plurality of memory devices.

12. (Amended) A memory module controller for [interfacing a plurality of memory device on a memory module with a system memory bus coupled to a

system memory module, the memory module controller] providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:

means for receiving from the system memory [bus] controller a first memory transaction [having] in a first format; and

means for [generating] converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction [corresponds to the first memory transaction and has a second format] is different [than] from the first format of the first memory transaction.

13. (Amended) A memory module controller ~~for~~ [interfacing a plurality of memory devices on a memory module with a system memory bus coupled to a system memory module, the memory module controller] for providing an interface between a system memory controller and a plurality of memory devices on a memory module comprising:

first interface circuitry configured to receive from the system memory [bus] controller a first memory transaction in a first format; and

control logic coupled to the first interface circuitry and configured to reformat [reformatting] the first memory transaction [transactions] such that [for] the plurality of memory devices perform the reformatted first memory transaction.